Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A process of fabricating an integrated circuit ~~manufacturing a semiconductor feature for use in a semiconductor device~~, comprising:

forming an opening in a substrate through a patterned photoresist layer and a hardmask layer located over said substrate with a plasma;

trimming said photoresist layer with a plasma to create an exposed portion of said hardmask layer;

removing said exposed portion with a plasma to create a trench guide opening; and

after removing said exposed portion, creating a trench through said trench guide opening with a plasma.

2. (Currently Amended) The process as recited in Claim 1 wherein forming said opening ~~includes~~ comprises patterning an opening through a bottom anti-reflective coating (BARC) layer located between said photoresist and said hardmask layer and a pad oxide located between said substrate and said hardmask layer.

3. (Original) The process as recited in Claim 1 wherein said hardmask layer is a silicon nitride layer.

4. (Original) The process as recited in Claim 1 wherein said forming, said trimming, said creating, and said removing are conducted in a same plasma tool.

5. (Currently Amended) The process as recited in Claim 1 further comprising ~~including~~ forming an oxide liner in said trench.

6. (Currently Amended) The process as recited in Claim 5 furthering comprising ~~including~~ depositing an oxide in said trench to form an isolation structure.

7. (Currently Amended) The process as recited in Claim 6 further ~~including~~ comprising removing said hardmask subsequent to forming said isolation structure.

8. (Currently Amended) The process as recited in Claim 1 wherein said trimming comprises ~~includes~~ trimming with a plasma having a source power ranging from about 300 watts to about 700 watts, a bias power ranging from about 0 watts to about 150 watts.

9. (Currently Amended) The process as recited in Claim 8 wherein said trimming comprises ~~includes~~ using gases including HBr, O_2, and Ar and a flow rate of each of said gases ranges from about 20 sccm to about 80 sccm.

10. (Currently Amended) The process as recited in Claim 1 wherein creating said trench comprises ~~includes~~ forming said trench adjacent an active region of said substrate.

11. (Currently Amended) A process of manufacturing an integrated circuit, comprising:

forming an isolation structure on a substrate adjacent an active region of said substrate, comprising: ~~including:~~

forming an opening in a substrate through a patterned photoresist layer and a hardmask layer located over said substrate with plasma;

trimming said photoresist layer with a plasma to create an exposed portion of said hardmask layer;

removing said exposed portion with a plasma to create a trench guide opening; and

after removing said exposed portion, creating a trench through said trench guide opening with a plasma;

forming transistors on said active region; and

forming interconnects in dielectric layers located over said transistors, said interconnects interconnecting said transistors to form an operative integrated circuit.

12. (Currently Amended) The process as recited in Claim 11 wherein forming said opening comprises ~~includes~~ patterning an opening through a bottom anti-reflective coating (BARC) layer located between said photoresist and said hardmask layer and a pad oxide located between said substrate and said hardmask layer.

13. (Original) The process as recited in Claim 11 wherein said hardmask layer is a silicon nitride layer.

14. (Original) The process as recited in Claim 11 wherein said forming an opening, said trimming, said creating, and said removing are conducted in a same plasma tool.

15. (Currently Amended) The process as recited in Claim 11 further comprising ~~including~~ forming an oxide liner in said trench.

16. (Currently Amended) The process as recited in Claim 15 furthering comprising ~~including~~ depositing an oxide in said trench to form said isolation structure.

17. (Currently Amended) The process as recited in Claim 16 further comprising ~~including~~ removing said hardmask subsequent to forming said isolation structure.

18. (Currently Amended) The process as recited in Claim 11 wherein said trimming comprises ~~includes~~ trimming with a plasma having a source power ranging from about 300 watts to about 700 watts, a bias power ranging from about 0 watts to about 150 watts.

19. (Currently Amended) The process as recited in Claim 18 wherein said trimming comprises ~~includes~~ including HBr, O_2, and Ar and a flow rate of each of said gases ranges from about 20 sccm to about 80 sccm.

20. (Currently Amended) The process as recited in Claim 18 [1] wherein forming said transistors comprises ~~includes~~ forming wells and source and drain regions in said active region.